Enabling low-power MAPS-based space trackers: a sparsified readout based on smart clock gating for the High Energy Particle Detector HEPD-02

Ricciarini S.B.[1], Beolé S.[2], de Cilladi L.[2], Gebbia G.[3], Iuppa R.[3], Ricci E.[3], Zuccon P.[3]

[1]IFAC-CNR, Firenze, Italy; [2]University and INFN, Torino, Italy; [3]University and TIFPA, Trento, Italy

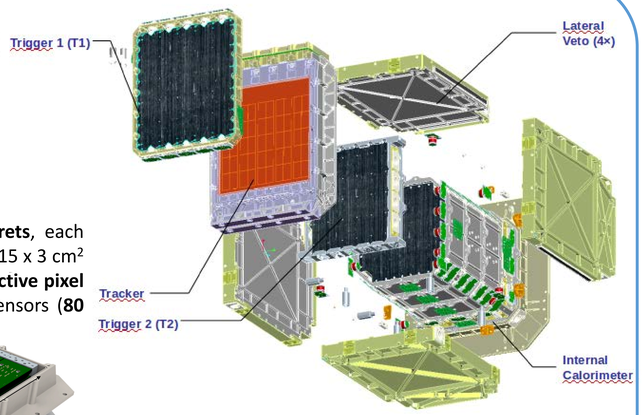
Abstract

The adoption of pixel sensors for space-based tracking detectors requires low power consumption and enhanced heat dissipation to cope with the satellite power and cooling constraints. The High Energy Particle Detector (HEPD) tracker onboard the CSES-02 will be the **first application of monolithic active pixel sensors (MAPS) to a satellite-based experiment**. This result is achieved with a parallel sparsified readout architecture implemented on a single low-power FPGA chip, which manages the 150 ALPIDE chips of the three-plane tracker. The power consumption is reduced by reading out the ALPIDE chips via the control line instead of the high speed data link, and by distributing the clock only to the portions of the detector crossed by a particle. The readout concept presented in this contribution allows to deal with both the required performance and the power constraints, and is scalable to larger and more complex detectors.

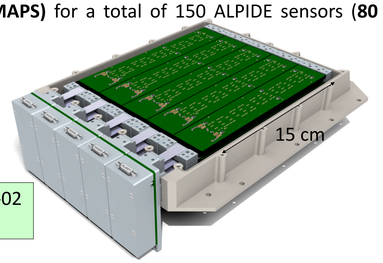
The HEPD-02 tracker

HEPD-02 is one of the payloads that will equip the **China Seismo Electromagnetic Satellite** (**CSES-02**) to be launched by end of 2022, aimed at measuring the flux of particles trapped in the terrestrial magnetosphere through calorimetry (scintillators) and tracking measurements of **electrons** between **3 and 100 MeV** and **protons** between **30 and 200 MeV**.

The **HEPD-02 tracker** is composed of **5 turrets**, each made of 3 planes or "staves" with active area 15 x 3 cm^2 each. A **stave** houses 10 **ALPIDE monolithic active pixel sensors (MAPS)** for a total of 150 ALPIDE sensors (**80 Mpixels**).



The HEPD-02 apparatus (exploded view).

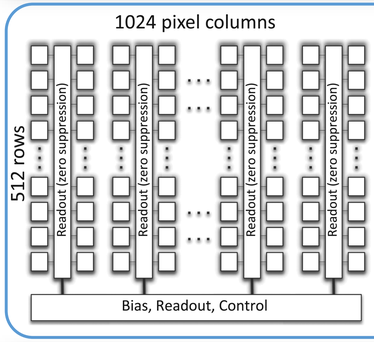


The HEPD-02 tracker.

On each stave, the 10 ALPIDE chips are positioned on a CFRP mechanical support and covered by a custom-designed **FPC (Flexible Printed Circuit)** connected to the chips via triple-redundancy bondings, for signal and power routing.
A custom-designed **TSP (Tracker SPlitter) compact PCB is positioned on the turret side** for cabled interface with power and control/readout electronics. The FPC/TSP connection is made via soldered wires (few cm length).

A tracker stave: the FPC and soldered wirings toward TSP are clearly visible.

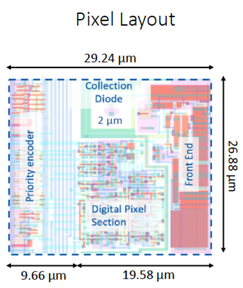
The ALPIDE MAPS in space



Structure of the ALPIDE chip.

The ALPIDE chip, developed by the ALICE collaboration at LHC (CERN), is made of 512 x 1024 pixels with 27 µm x 29 µm pitch on an area of 15 x 30 mm^2.
The analog in-pixel front-end circuit gives **binary zero-suppressed output**.
The ALPIDE chip contains an overall readout and control digital circuit which implements a **sparsified readout** with data from only the hit pixels.

The use of ALPIDE in HEPD-02 constitutes **the first space application of MAPS**. Compared to the traditional hybrid microstrip sensors employed in previous space experiments, MAPS enable **higher granularity, low noise, compact assembly** (with sensor and front-end circuit on the same Si substrate) with **much fewer bonding interconnections;** last but not least, production costs are lower.



Structure of the ALPIDE pixel.

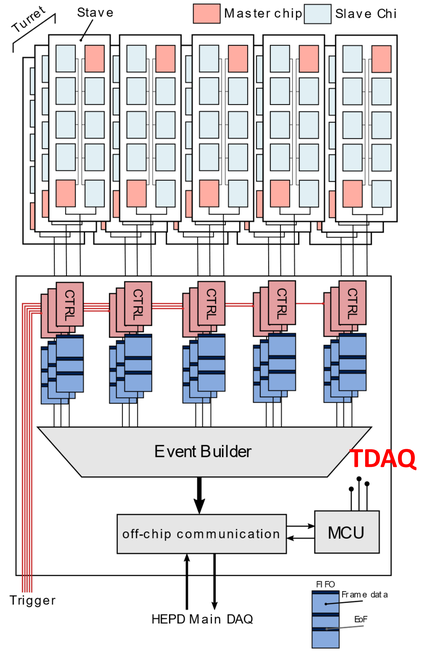
Low-power readout architecture

The satellite application imposes a **strong design optimization effort in terms of power**, to match the **budget constraints** (~16 W available for the whole tracker, including the readout electronics) and to allow for an adequate **cooling in vacuum** (with no air convection) by pure conduction through the stave CFRP toward the external Al-alloy frame.
An application-specific **low-power parallel readout architecture** has been therefore implemented, with several changes with respect to the one designed for ALICE detector at CERN.

- **ALPIDE master-slave architecture**. Each stave contains two chains of 5 chips with one master each. The readout of the 4 ALPIDE slaves is made by the master through a local 80 Mbps bus.
- **ALPIDE master readout through serial slow-control line** (up to 40 Mbps). The ALPIDE built-in fast data transmission unit (DTU, 1.2 Gpbs) is kept permanently switched-off; the external readout is implemented via the slow-control line instead.

With such configuration, the maximum power consumption for each ALPIDE chip amounts to **55 mW** (to be compared with up to 150 mW in the application at CERN). Correspondingly, the dead time is increased but still acceptable for the HEPD-02 application, given the relatively low trigger rate sustainable by the system as a whole (up to few kHz, varying along the orbit).

- **Minimal external control and readout electronics.** The whole tracker control and readout is managed by a single fully customized board (TDAQ) interfacing with the central unit of the HEPD-02 system and implementing only the necessary functionalities to fully assure the required tracker operation and performance. The TDAQ board contains a single Xilinx Artix 7 FPGA with auxiliary flash EEPROM and SRAM memories, with a power consumption matching the 3 W allowable budget.



- **Clock gating:** ALPIDE clock is normally kept off, set on only as a response to a particle trigger from the HEPD-02 scintillator system and only for the time necessary for event readout.
- **Dynamic scaling of clock frequency:** the clock frequency can be dynamically reduced in regions of the orbit where the trigger rate is significantly lower (i.e. when the satellite is out of the Van Allen belts) and an increase of data readout dead time is therefore acceptable.
- **Segmentation of the first HEPD-02 trigger plane in 5 bars**, each one set on top of a tracker turret. This allows to distribute the clock signal **only to the turret below the activated trigger bar and to the adjacent ones.**