Improving RF Detectors with Programmable Logic

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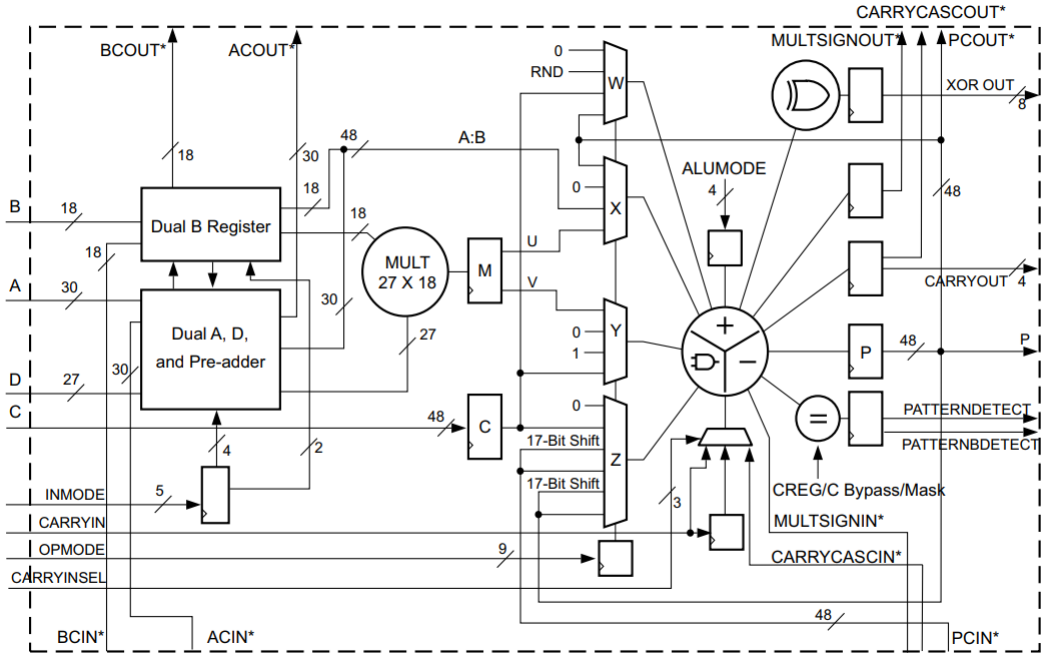
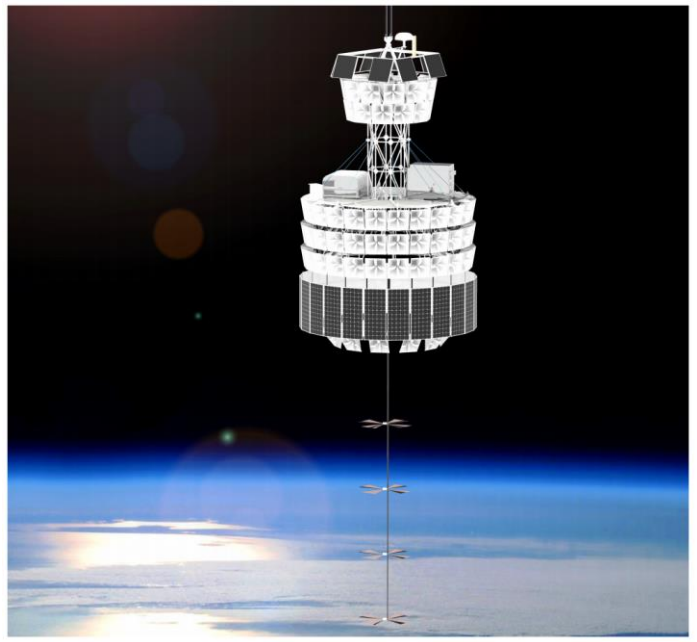
University College London



Digital Signal Processing
slice on RF-system-on-chip

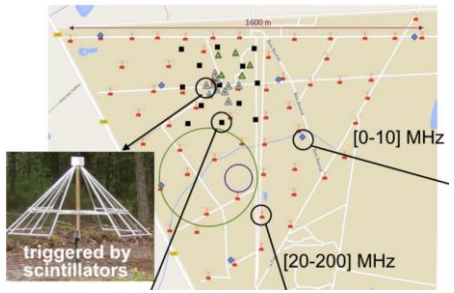


PAYLOAD FOR ULTRAHIGH
ENERGY OBSERVATIONS

Motivations

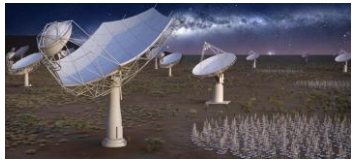
Several channels with sub-GHz radio frequencies:
- Neutrino in ice (Askaryan)
- Cosmic ray or tau extensive air showers

Beamforming <u>at trigger</u>:
- Significant benefit if detection is trigger threshold limited
- Programmable logic naturally suited to purpose

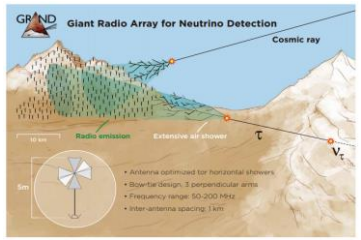


CODALEMA / EXTASIS: radio array triggered by particle detector

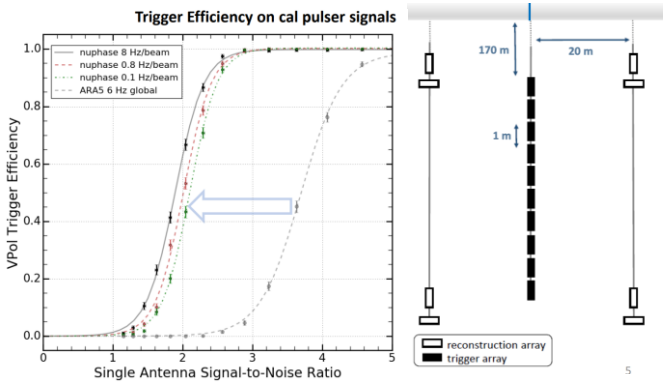
LOFAR: measure CR-induced radio emissions, 30-80Mhz



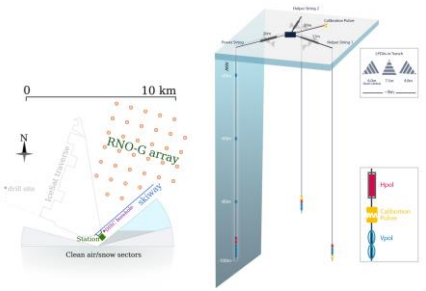
Square Kilometre Array



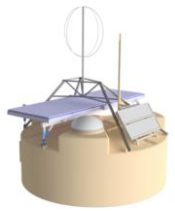
GRAND & protoGRAND



Installed: ARA5 station with NuPhase interferometric trigger

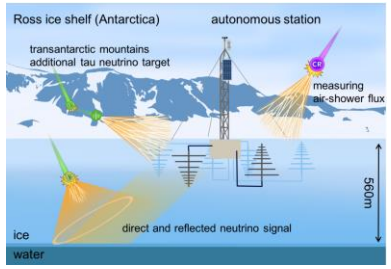


In progress: RNO-Greenland with interferometric trigger

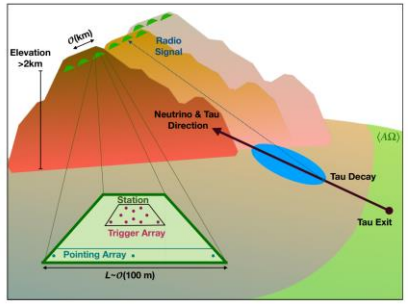


AugerPrime / Auger Engineering Radio Array

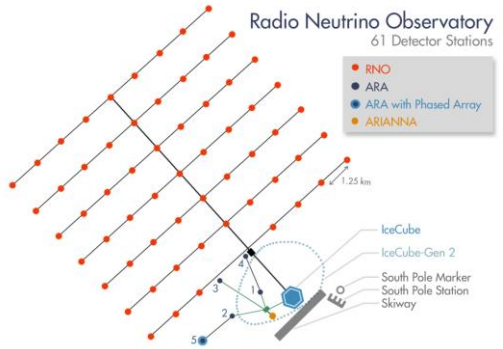
IceTop (IceCube) radio extension

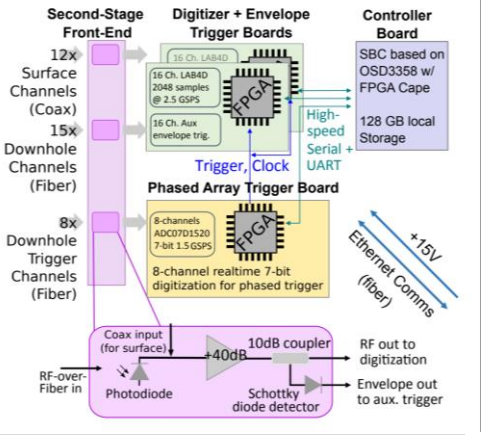


ARIANNA: seven 4-channel arrays installed



Proposed: high elevation neutrino radio detection with beamforming radio array





Proposed: Radio Neutrino Observatory
8 channel phase array trigger (related: IceCube-Gen2)

Why beamforming…

N Antenna Sum

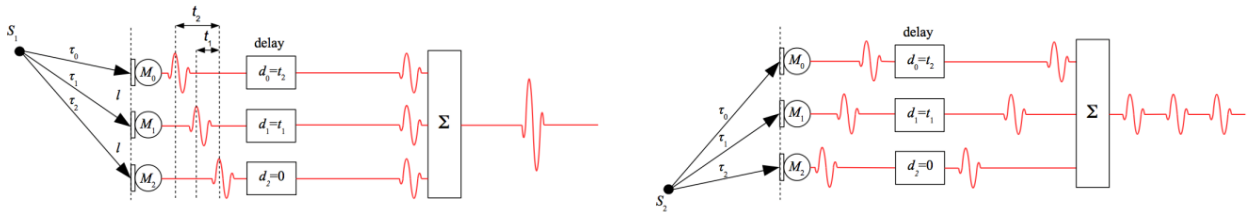
Thermal noise
(uncorrelated between antennas) → Scales as √N

Signal
(correlated between antennas) → Scales as N

Signal to noise ratio → Improves by √N

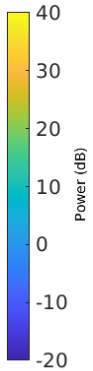
➔ Improves detector sensitivity

Geometry requires ‘delay and sum’

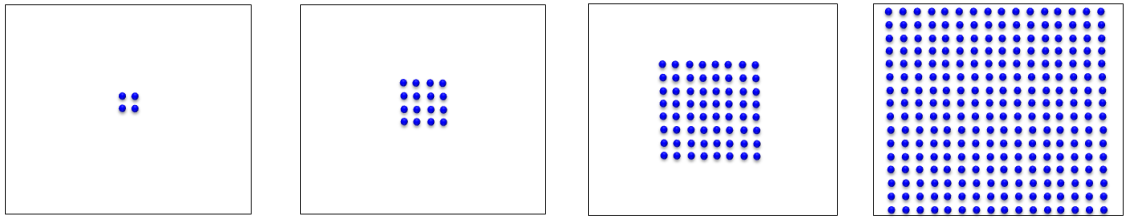


Directionality ➔ array of ‘beams’

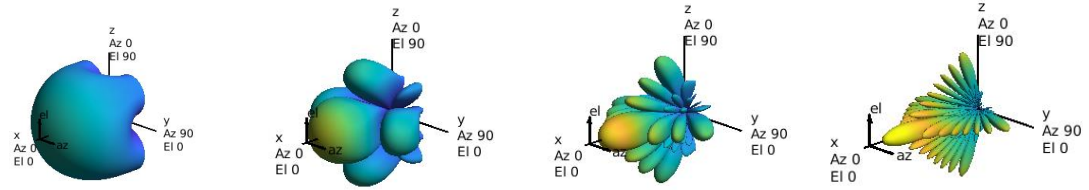
- Increases with number of antenna per sum



2D array pattern



Beam power

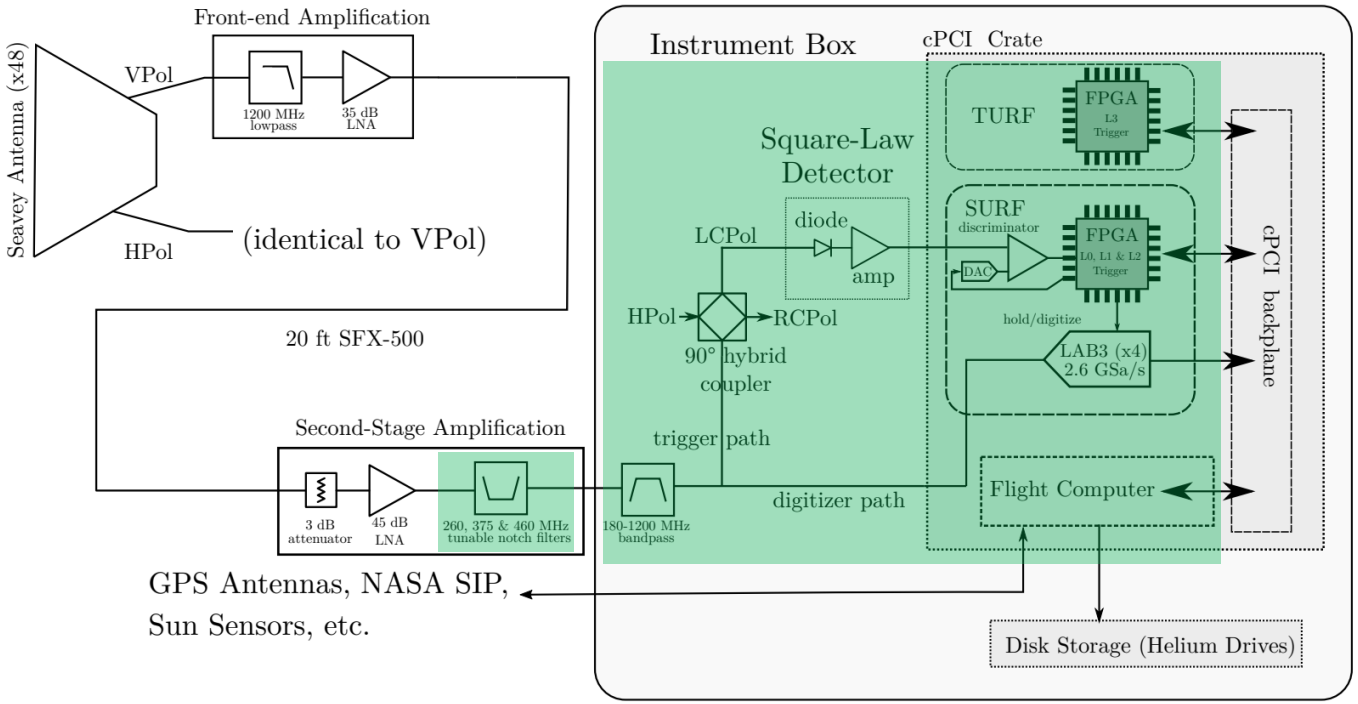


➔ Significant computational resources

Why digital beamforming with RFSoC…

Combine functionality of analogue components
- ✓ Reduced power
- ✓ Increased computational capacity
- ✓ Reconfigure in-flight

ANITA-IV Block Diagram

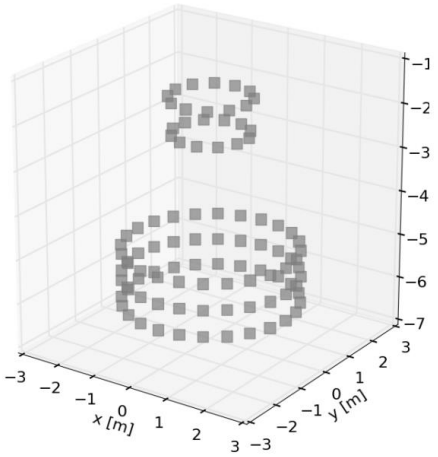


Xilinx Radio-frequency-System-on-chip:
- FPGA + 8-16 digitisers (+ more)
- 12-14 bit
- 4-6 GHz
- 4000+ digital signal processing slices

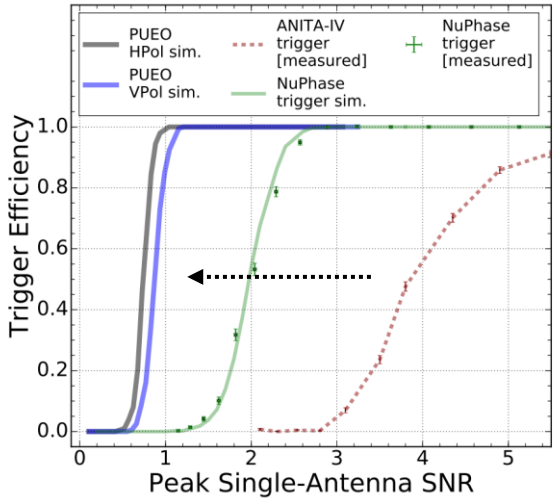
Concrete application – PUEO

PAYLOAD FOR ULTRAHIGH ENERGY OBSERVATIONS – evolution of the ANITA experiments

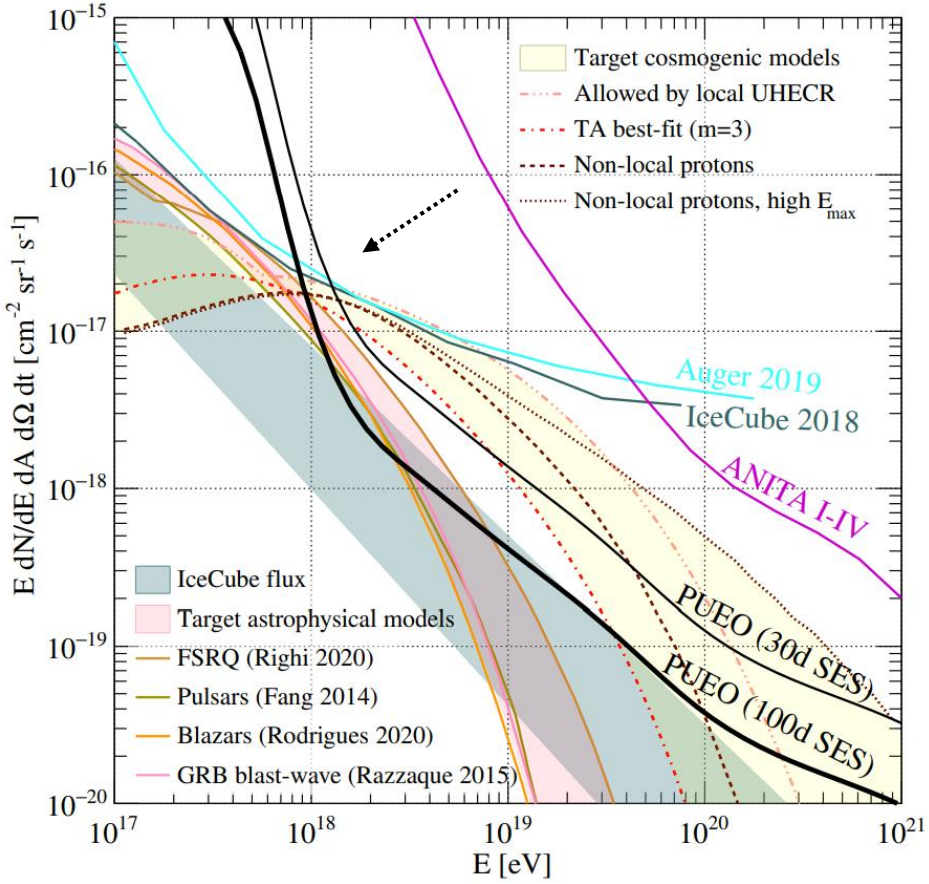
216 antennas
Sensitive to air showers and Askaryan channels



5x lower energy threshold vs. ANITA



Enhanced ultra high energy neutrino sensitivity



Want to…

I. Demonstrate on hardware
II. Quantify resources
III. Improve performance
IV. Digital filtering?

arxiv 2010.02892

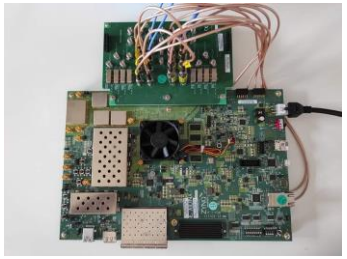
I. Demonstrate on hardware

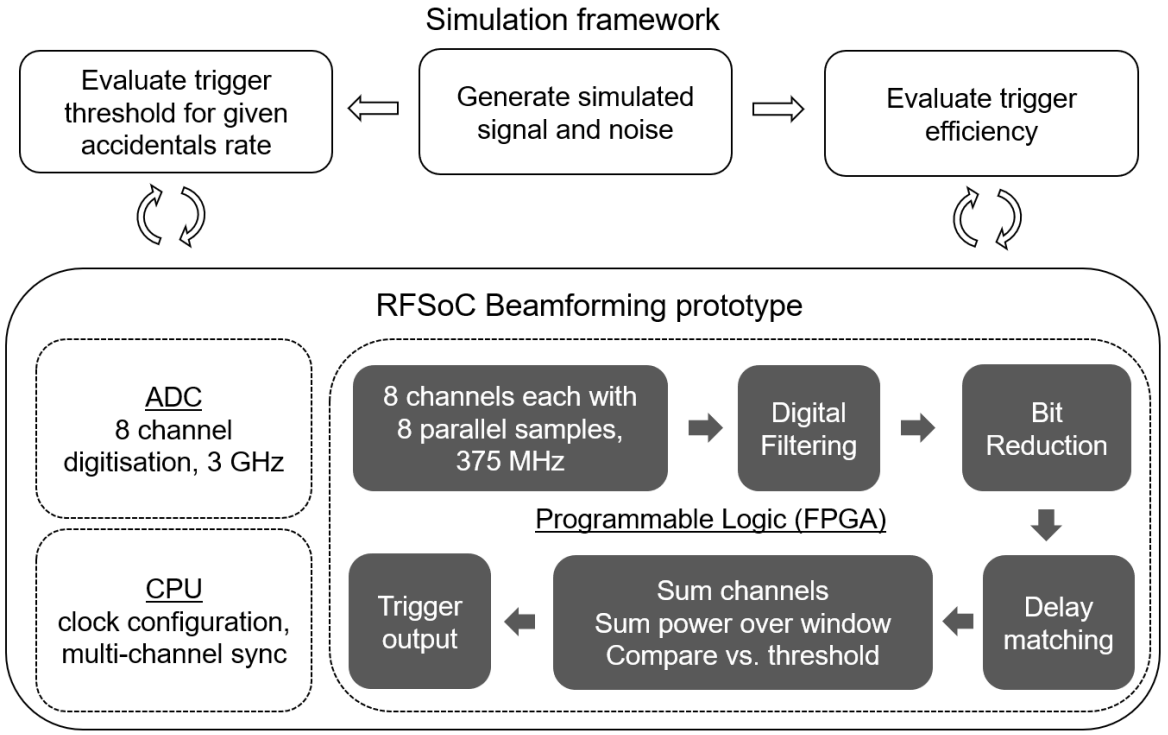
Beamforming prototype

Programmable logic
- Xilinx tools, hardware description language

Software for on-board CPU
- Program clocks + generate simulated signal/noise

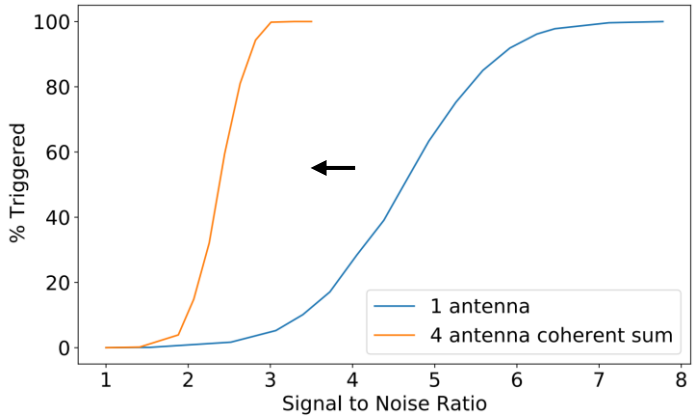
8 parallel samples per clock cycle
- 3GHz digitisation + 375MHz FPGA





Performance

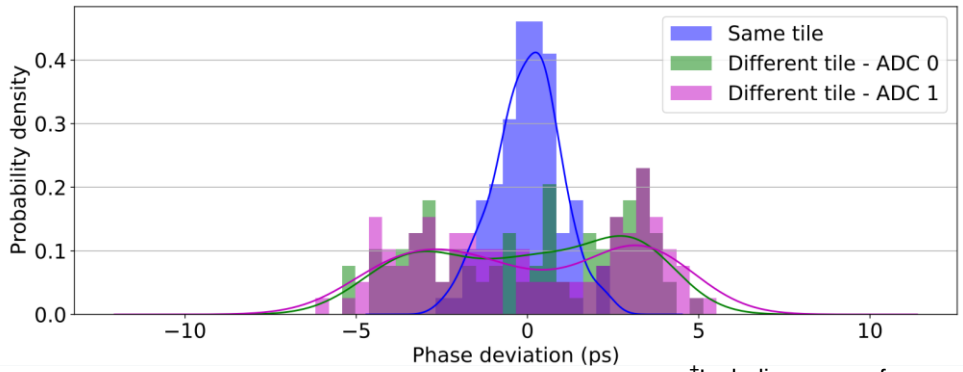
Demonstrates beamforming improvement for trigger threshold*



*limited to 4 channels due to evaluation board limitation

Channel alignment

Cross channel phase jitter under 0.01ns† ≪ 0.33ns sample period



†Including across frequencies

II. Resources

PUEO requires ~100 beams per RFSoC

RFSoC can accommodate this

Resource utilisation*

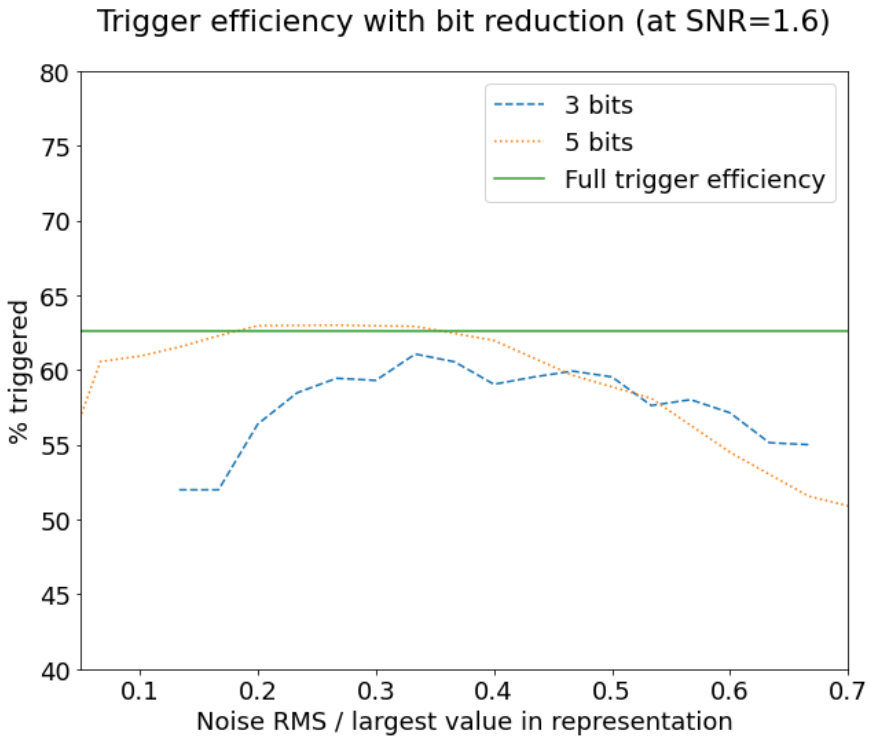
100 beams

	DSP	CLB
12 bits	10%	25%
5 bits	5%	10%
3 bits	5%	6%

- 8 parallel samples increases resource usage
- Includes resource improvements from Carry-Save: efficient multiple-number addition using single DSP
- significant savings through bit reduction

*8 channels and 8 samples per clock cycle
DSP = Digital Signal Processing slices
CLB = Configurable Logic Blocks
As % of available resources on Xilinx ZU28DR device

Bit reduction



Sensitive to scaling vs. dynamic range

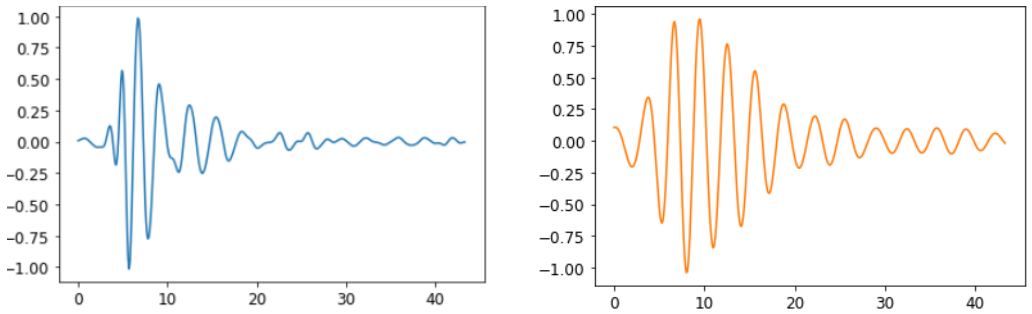
Trigger efficiency unaffected at 5 bits

- Small loss in fidelity at 3 bits

III. Optimising beamforming efficiency

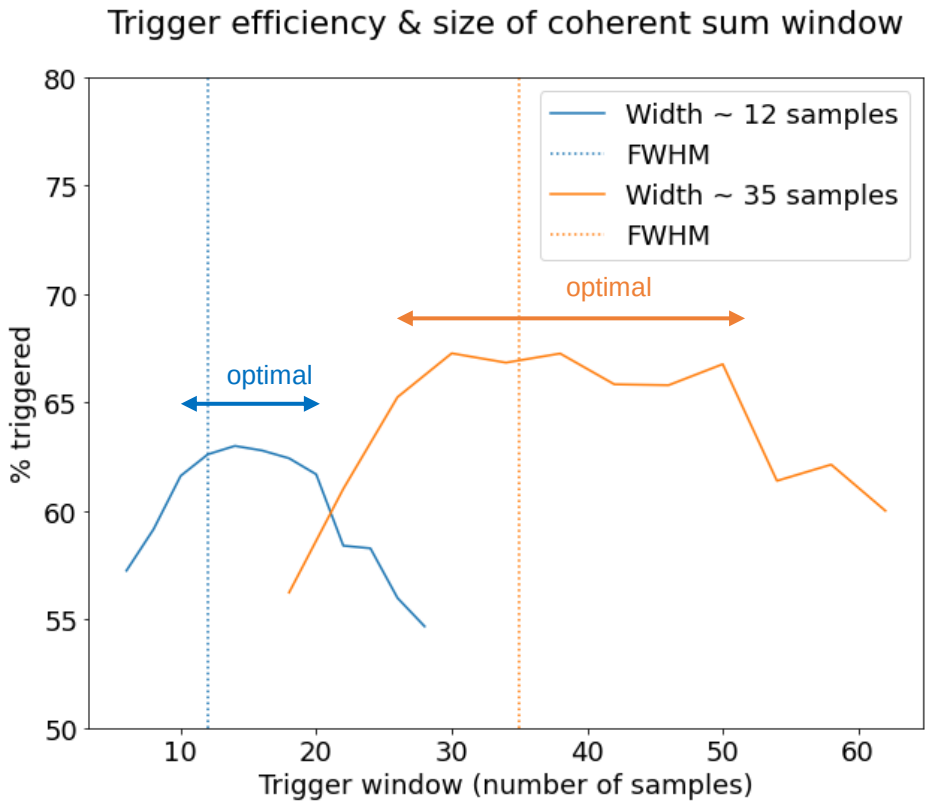
Duration of coherent sum window

Signal dependent driver of trigger performance



- Full-width-half-maximum is roughly optimal

Wide range of signal widths could mean no single optimal window size

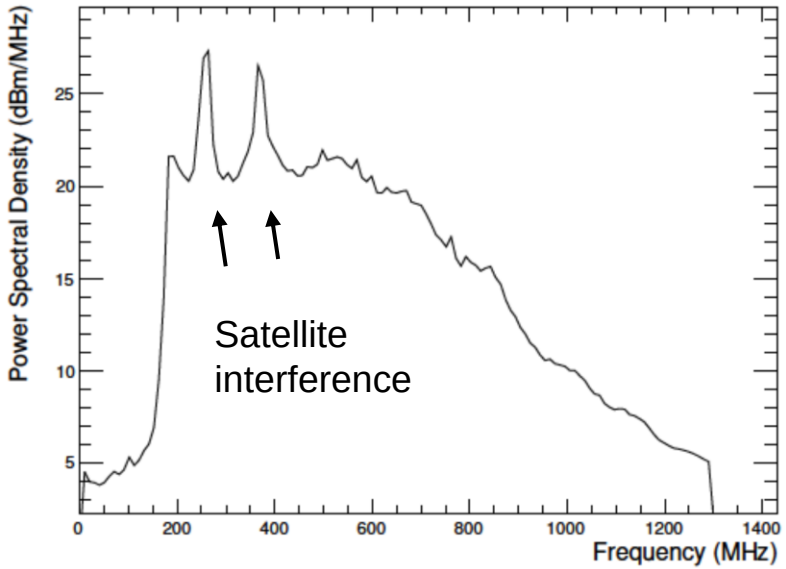


Other drivers of performance:

- Stepping between adjacent windows
- Round vs. truncate for bit reduction

IV. Filtering

ANITA-III flight snapshot



arxiv 1709.04536

Increases beamforming sum ➔ reduced trigger sensitivity

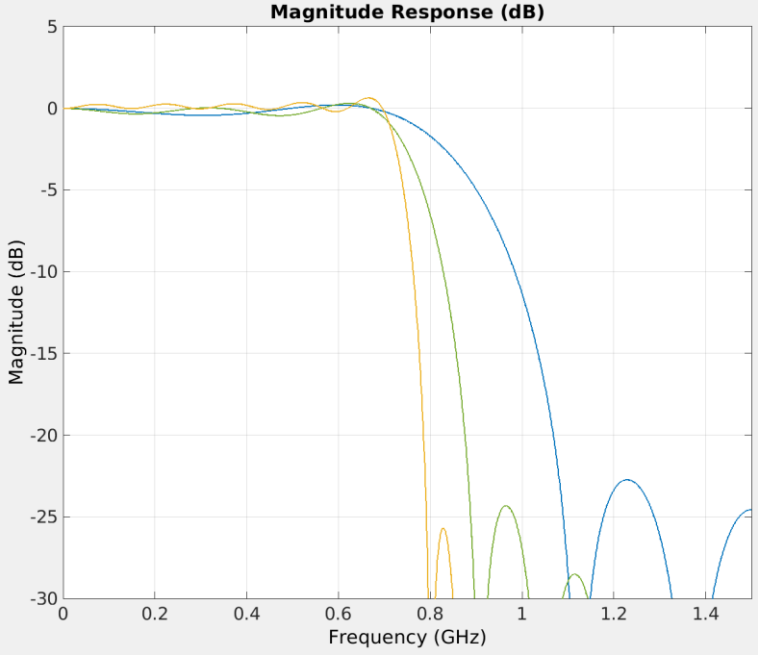
Do not know sources before flight

Impact also dependent on field of view

Want tunable filters – programmable logic!

IV. Filtering – examples

FIR (finite impulse response) filters
- Simple to implement
- Linear phase response – no shape distortion
- Resource expensive



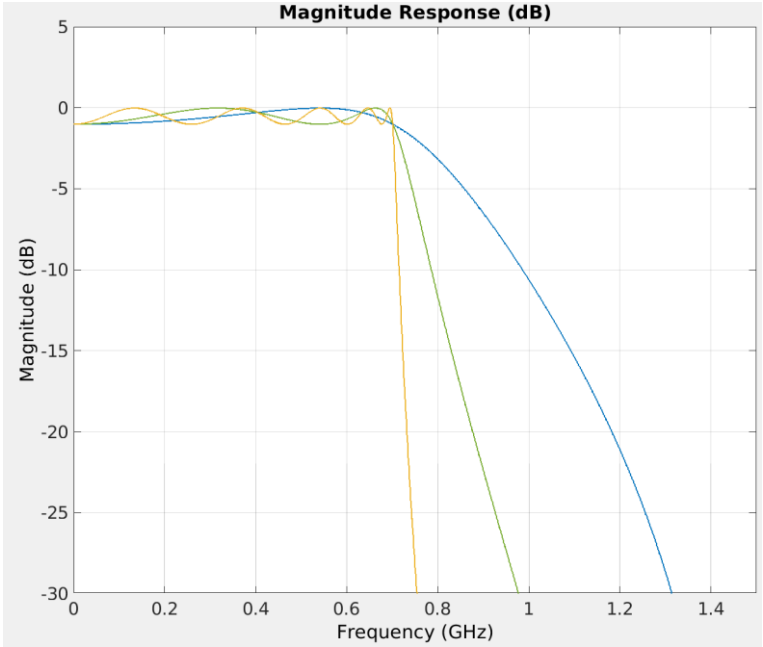
1: Low pass filter

FIR suited for low/high pass filters, if sharply falling response not required

DSP utilisation per filter*

Utilisation	Width to -10dB	
	FIR	IIR
10%	280MHz	280MHz
20%	130MHz	85MHz
40%	60MHz	15MHz

IIR (infinite impulse response) filters
- Non trivial to implement
  - Parhi & Messerschmitt (1989)
- Shape distortion
- Fewer resources – use if need steep response



*~4000 DSPs per RFSoC. 8 channels and 8 samples per cycle. No symmetries assumed except for symmetric FIR taps, so additional resource reduction possible

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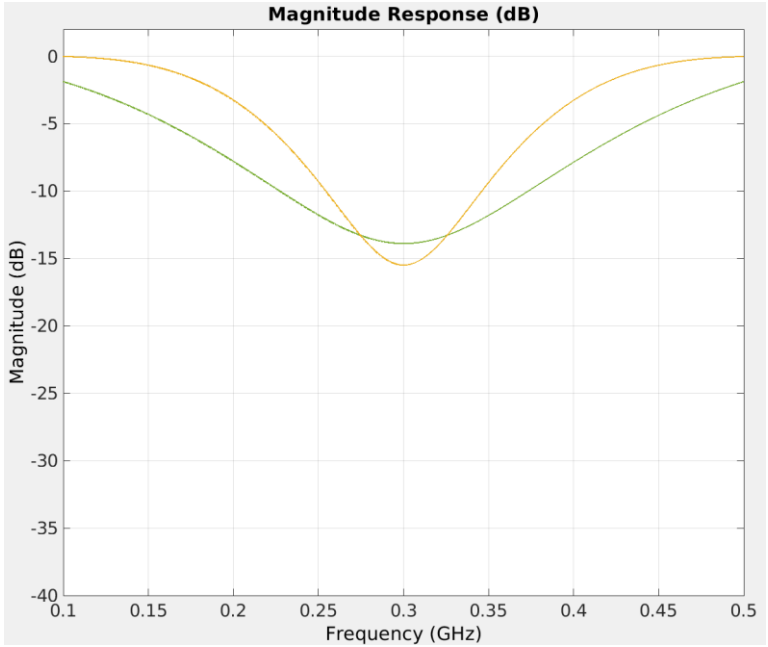


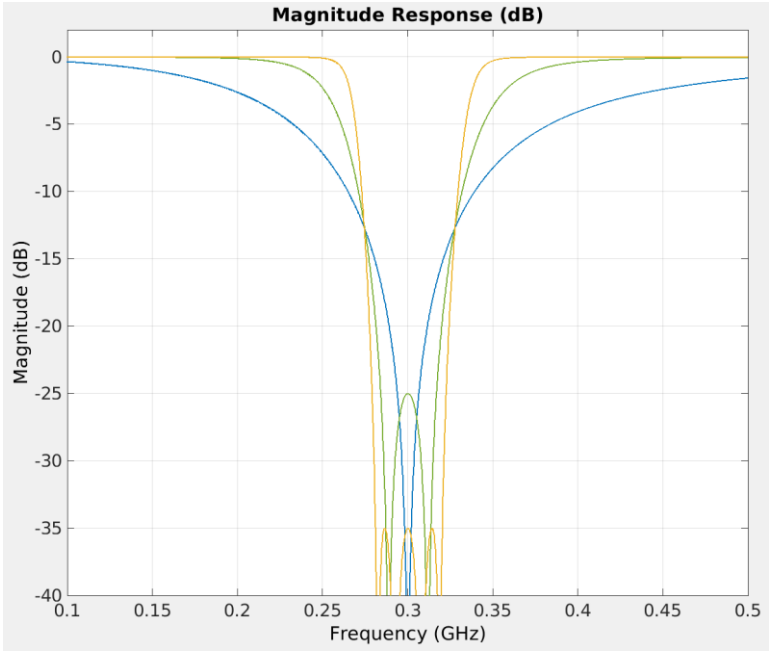
2: Notch filter

IIR likely necessary for notch filters, as steeply falling response required

DSP utilisation per filter*

Utilisation	Width to -2dB	
	FIR	IIR
10%	N/A	230MHz
20%	340MHz	60MHz
40%	180MHz	15MHz

IIR (infinite impulse response) filters
- Non trivial to implement
  - Parhi & Messerschmitt (1989)
- Shape distortion
- Fewer resources – use if need steep response



*Require 50Mhz, -13dB stopband at 300Mhz. ~4000 DSPs per RFSoC. 8 channels and 8 samples per cycle.

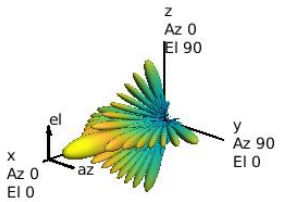
Summary

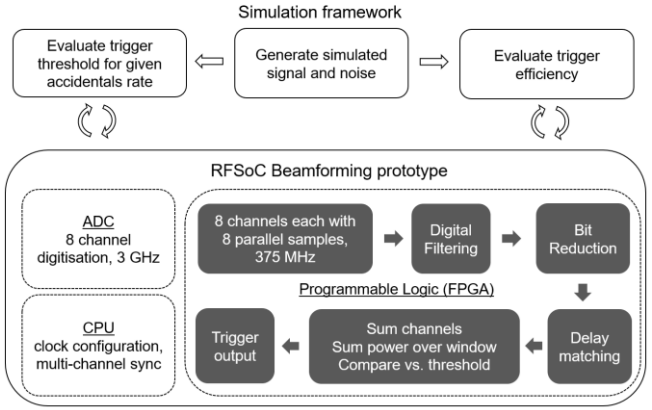
Digital Beamforming:

- √N trigger threshold improvement
- Computation-intensive
- RFSoCs - low power, high performance
- 5x improvement in PUEO energy sensitivity

Capabilities & Optimisations

- Adequate resources for beamforming
- Bit reduction + carry-save to minimise resource usage
- Low/high pass and notch filters with in-flight tuning





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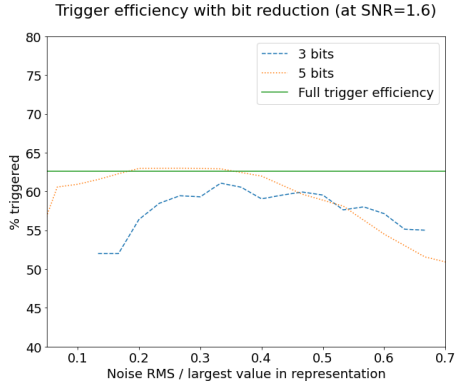
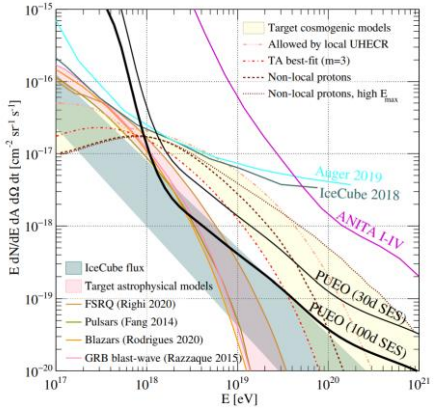
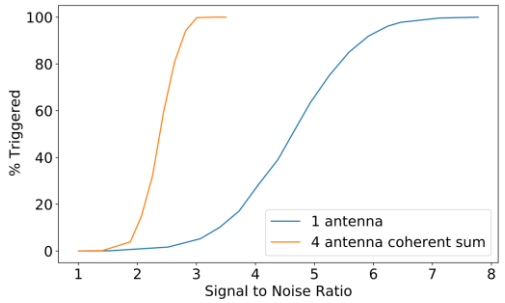
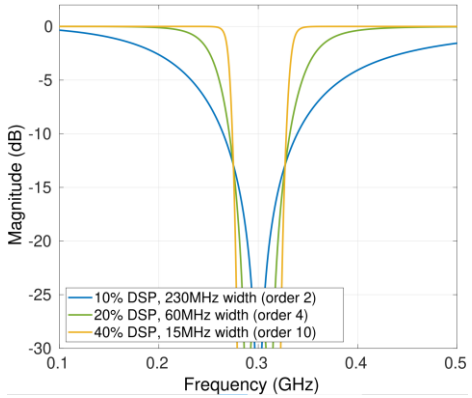






IIR notch filters



FIR low pass filters