An Advanced Triggerless Data Acquisition System for GRAPES-3 Muon Detector

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Abstract

The large area 560 m² directional muon telescope at Gamma Ray Astronomy at PeV Energies phase-3 (GRAPES-3) experiment in Ooty, India was designed primarily to study the extensive air showers (EAS) and made operational in year 1998. It has turned out to be an unique instrument to make fascinating study of exotic phenomenon by introduction of a new parallel data acquisition system (DAQ) in year 2000 to measure the muon directional flux. The recent discoveries of transient weakening of Earth's magnetic shield probed by a Cosmic Ray Burst and measurement of the electrical properties of a thundercloud through muon imaging has demonstrated the capabilities of this instrument. The design of new triggerless muon data acquisition system (TM-DAQ) using Field-programmable gate array (FPGA) would enhance the present capabilities and open a new window on several physics fronts such as, a) precise measurement of the muon flux for thunderstorm studies, b) study of large angle EAS using the muon component, c) search for exotic particles characterized by early or delayed arrivals. We present here the key salient features of the TM-DAQ along with initial observations.

The GRAPES-3 existing Muon Detector System





Fig. 1: Schematic view of a PRC

• Proportional counter (PRC), dimension 600 X 10 X 10 cm³ as muon detector • Total 3712 PRCs, arranged in 16 muon modules covering an area of 560 m² • 2 m thick concrete blocks as absorber provides energy threshold of ~1GeV • Present DAQ has large dead time, obsolete interface techniques, coarser data recording thus limiting the scope of new science



Firmware for Triggerless Muon DAQ System (TM-DAQ)





Salient <u>Features</u>

Fig. 7: Block diagram representing firmware embedded in FPGA for TM-DAQ

- State Machine based design approach
- Continuous monitoring and recording of all Hardware parameters (HWM)
- Control Word Exchange (CWE), establishes a faithful communication between device & PC
- Smart Auto Reset feature for both device and PC using HWM.
- Signal Validation Module (SVM) checks integrity for all I/P signals
- Trigger module (TRIG) generates Layer-OR and coincidence between layers
- Pulse width and timing (PWT) measures arrival time and pulse width for all valid inputs with a resolution of 10 nsec and records in DDR
- Count rate mon monitors rate for all I/P and triggers and records in DDR

Fig. 3: Block diagram representing existing DAQ for a muon module

- DDR module utilises the onboard DDR in ping-pong mode and has capacity to store 256Mbits/sec
- GPS corrected real time clock (RTC) resolution 10 nsec
- Board to board (B2B) modules shares the TRIG O/P between Master-Slave
- SPI enables smooth transfer of data from Slave board to PC via Master
- FTDI modules provides bidirectional communication between PC and Master
- Integrated temperature recording (TEMP) for onboard crystals

Hardware for Triggerless Muon DAQ System (TM-DAQ)

Salient Features

- Negligible dead time (~0.001% compared to 15-20% for the legacy DAQ system)
- Simultaneous measurement of precision pulse width and arrival time for all inputs with a resolution of 10 ns
- Excellent time matching between various cards, allowing to implement offline trigger condition





TM-DAQ Installation and Observations

• TM-DAQ installed for 4 muon modules - 928 PRCs in parallel to existing system



The measured flux from the TM-DAQ (b) is larger by ~20% as compare to the existing DAQ (a) which is a significant improvement

Precise measurement of the would flux enhance muon thunderstorm studies

Figure 8: Muon flux measured using 4-fold trigger (a) Existing DAQ (b) TM-DAQ

Fig. 4: Block diagram representing hardware of TM-DAQ for a muon module

Fig. 5: ALICE board mounted on **Interface Card**

- ALICE Board The board is a High-Level-Trigger (HLT) Read-Out Receiver Card (H-RORC) used for ALICE detector at LHC Point 2, CERN Geneva during Run I phase
- FPGA XILINX make Virtex4 XC4VLX40- 1no., DDR 256Mbits 4 no.
- 2 numbers of onboard crystal for generating clock of 100MHz and 50MHz
- Interface Card I/O Interface between ALICE board and GRAPES-3 system in terms of level translator, matching connectors and PC interface.
- A set of board configured as Master and Slave to process data from all 236 PRC's of a module
- Hardware for both master and slave is same. However master has additional firmware to support data transfer between the boards and PC
- Interface to PC is via USB-2.0 by using FTDI module on master



Figure 9: Pulse Width Spectrum for one of the PRC using TM-DAQ

In existing DAQ the pulse width spectrum (PWS) of each PRC was performed in a multiplex mode thus allowing to monitor the performance of the PRC only for duty cycle of 1.5% however, TM-DAQ allows continuous PWS for each PRC

A prominent single muon peak ~20 keV due to cosmic ray muons and self calibrating Fe and Zn peak at 6.4 keV and 8.6 keV respectively due to K-alpha X-ray emission

It is now possible to study the EAS at large angles through the muon component using TM-DAQ and details are presented by B. Hari Haran et al @ PoS(ICRC2021)379.

The measurement of precise arrival time with 10nsec resolution for each individual hits allows to make a detail study of the muon flux during thunderstorm studies which happens at time-scale of ms.