The HEPD-02 Data Processing and Control Unit for the CSES-02 mission

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ABSTRACT

The China Seismo-Electromagnetic Satellite (CSES) is a multi-instrumental space mission devoted to the study of the ionosphere, with the main aim to investigate possible correlations between fluctuations of the ionosphere environment and the occurrence of an earthquake. The first satellite (CSES-01) was launched on 2018, while a second one (CSES-02) is currently under development and the launch is expected by 2022. As CSES-01, the second satellite includes a particle detector (HEPD-02, High-energy Particle Detector) to measure the increase of the electron and proton fluxes due to short-time perturbations of the radiation belts induced by solar, terrestrial, or anthropic phenomena. The explored energy range is 3-100 MeV for electrons and 30-200 MeV for protons .
The HEPD-02 Electronic Subsystem (ELS) contains all the electronics that perform the control of the apparatus and the processing of the signals provided by the sensitive detectors. It consists of the following boards: Trigger, Tracker Data Acquisition (T-DAQ), and Data Processing and Control Unit (DPCU). The DPCU will carry out the functions of management and control of the HEPD-02 operations and the communication with the satellite computer. The DPCU board will implement HOT / COLD redundancy and rely on a Zynq XC7Z7045 Xilinx System on Chip (SoC). The boot and all the functional checks of the SoC will be carried out by a MICROSEMI ProASIC3E FPGA. We present the main DPCU characteristics and functionalities, highlighting the electronic architectural choices to guarantee reliability and radiation tolerance during the entire mission life span.

Image credit: NASA

INTRODUCTION

The High Energy Particle Detector (HEPD) is designed to detect electrons in the energy range from 3 to 100MeV and Protons in the range from 30 to 200MeV with good energy (at least 10% at E > 5 MeV) and angular resolutions (at least 10° at E > 3 MeV) . The DPCU is the HEPD-02 board responsible for carrying out all the activities of: control of the apparatus, reading of the event data coming from the Front-end boards (TRIGGER & T-DAQ), management of the interfaces towards the Onboard Data Handling Computer of the Satellite CSES, carry out housekeeping and diagnostics of the health of the apparatus.

THE DPCU board ARCHITECTURE

The DPCU board is based on HOT/COLD redundancy and is divided into three distinct areas HOT, COLD and COMMON. The HOT and COLD sections are identical and host the same hardware and architecture and they work in cold redundancy (active one at a time). In the board COMMON area there are all the circuits necessary for the lines impedance matching and the management of the interfaces which are common to both the HOT and COLD sections. As shown in Fig. 1, the electronics of the HOT (COLD) areas are based on a Zynq XC7Z7045 Xilinx (XC7Z045-L2FFG900I) System on Chip (SoC) flanked by a MICROSEMI ProASIC3E (A3PE) FPGA. The Xilinx SoC performs the task of control and processing unit while the A3P FPGA has the task of managing the boot of the SoC and performing the role of WatchDog (WD) of the SoC, verifying its correct functioning. To prevent SEU failures in the boot memory, the DPCU board is designed to allow the SoC boot from different boot devices on the board. All the memories on the board are protected with protection and recovery mechanisms (ECC,EDAC etc.).

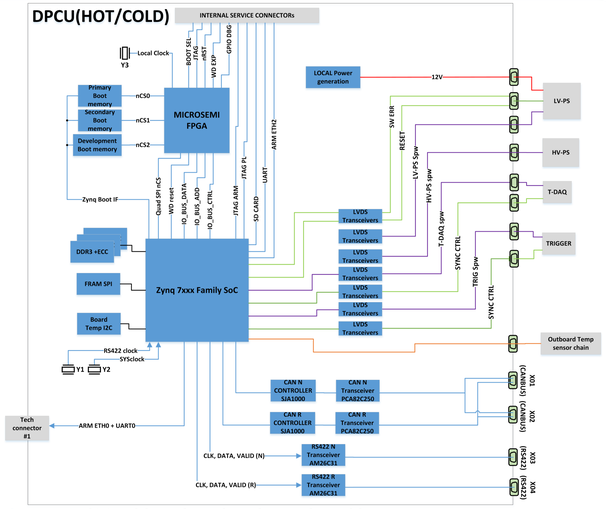

Fig. 1 : HOT(COLD) board section electronic architecture

THE DPCU board Interface

SPACEWIRE interfaces

The spacewire interfaces of HEPD-02 have been developed as an evolution of those present in HEPD-01. In the first detector the spacewire simply performed the task of slow control interface, while in the new device the interface performs the additional task of data transfer interface from the front-end cards to the DPCU. Reusing the architectural choice already experimented and tested in HEPD-01, the management of the four spacewire connections are implemented in the logical part of the SoC and the LVDS physical layers are created through the use of LVDS transceivers mounted on the board (Fig. 2).

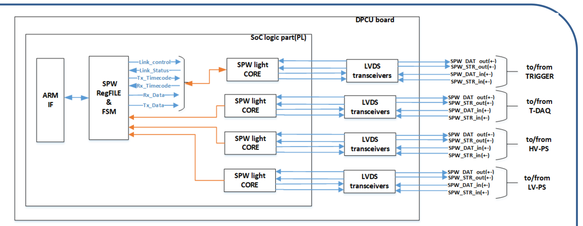

Fig. 2 : SPACEWIRE interface implementation

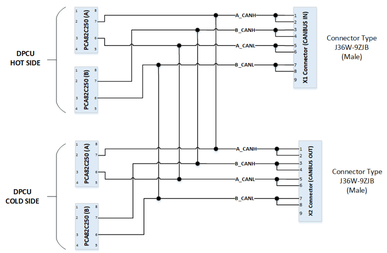

Fig. 3 : CANBUS interface interconnection scheme.

CANBUS Interface

The DPCU board is designed for the management of two CAN bus channels (CAN A and CAN B) with the CAN2.0 standard. As defined in the satellite requirements, in order to ensure redundancy, the board shall be able to manage communication on both channels but it will not have to communicate simultaneously on both CAN buses (Fig 3). The two CAN channels are one nominal and one redundant but always active. Communication from DPCU to satellite on the CAN channel occurs only after a query made by the satellite's OBDH computer.

RS-422 INTERFACES (scientific data bus)

The RS-422 interface of the DPCU board is dedicated to scientific data transfer to the satellite. This interface is developed as a unidirectional (write only) serial peripheral interface (SPI) protocol on a physical layer using an RS-422 transceiver. As defined in the satellite requirements this interface provides two links, one nominal and one redundant, which simultaneously transmit the data packets (Fig. 4). The physical layer use the transceiver texas instruments AM26C31 already used and validated in the HEPD-01 CPU board. The RS422 interfaces have a nominal clock of 6 (± 0.5%) MHz, a data frame transmission interval of T1 = 5.5 ms (MAX) and of inactivity equal to a time T2 = 10us (min).

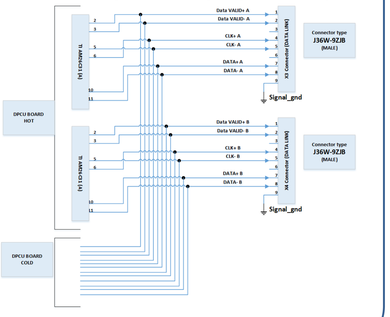

Fig. 4 : RS422 interface interconnection scheme.

WATCHDOG MANAGEMENT

In order to monitor and manage the correct status of the DPCU, the board is provided with two distinct watchdogs with different timings. A local watchdog is implemented directly on the DPCU board, while an external one is implemented on the CTRL-LV board. The external watch dog carries out a very important activity during the power-up phase of the device. The local watch-dog mechanism implemented on the DPCU board, on the other hand, has the task of detecting any problems on the programmable logics or on the software of the board. In case of any problem, the A3P FPGA signals the anomaly to the CTRL-LV board by asserting a SW_ERROR signal.

ELECTRONIC COMPONENT SELECTION

Given the high constraints imposed by ITAR on space-qualified components, their re-exportability and usability, and the non-critical radiation profile envisaged for the satellite, the selection of the DPCU board components was mainly carried out on commercial components off the shelf. This choice was also further driven by the good results of the studies on the usability of commercial components for non-critical space applications. Furthermore, for the design of the DPCU board, we tried to reuse as much as possible the components already present in HEPD-01, such as: transceivers, FRAM and FLASH memories.

CONCLUSION

The design of the board has been completed and its production will start shortly. The enormous flexibility of the architecture and the good computing power make the DPCU board a good tool which could be used in future missions.